

FIG 1A

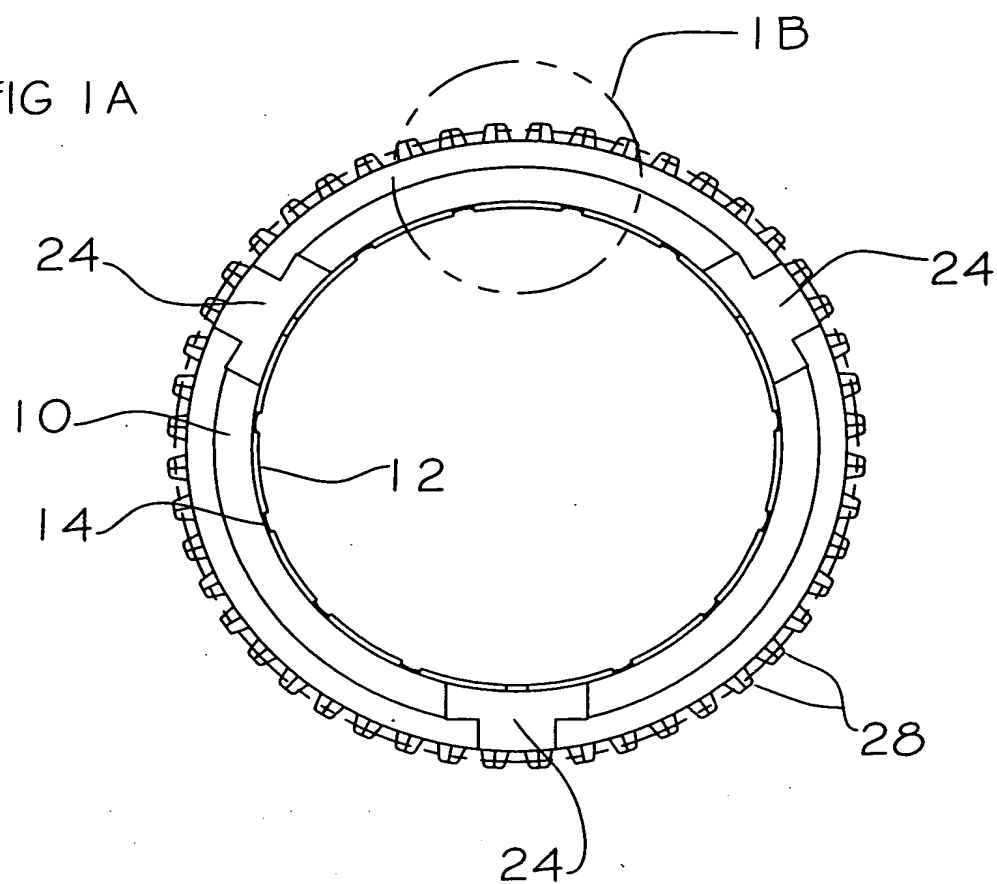
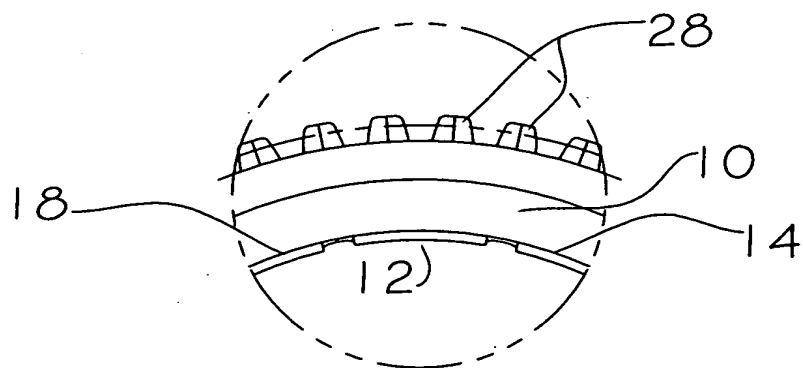


FIG 1B



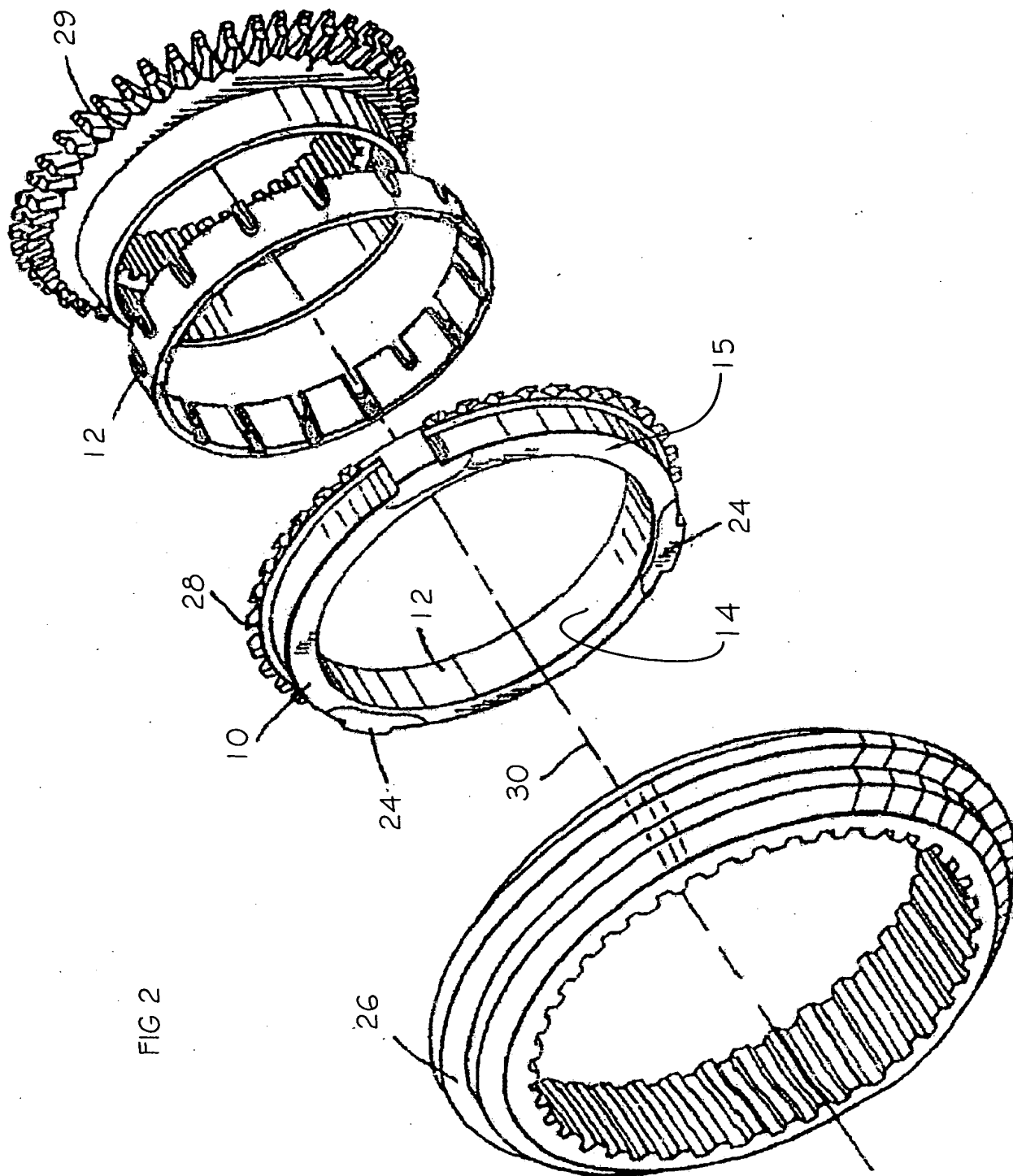
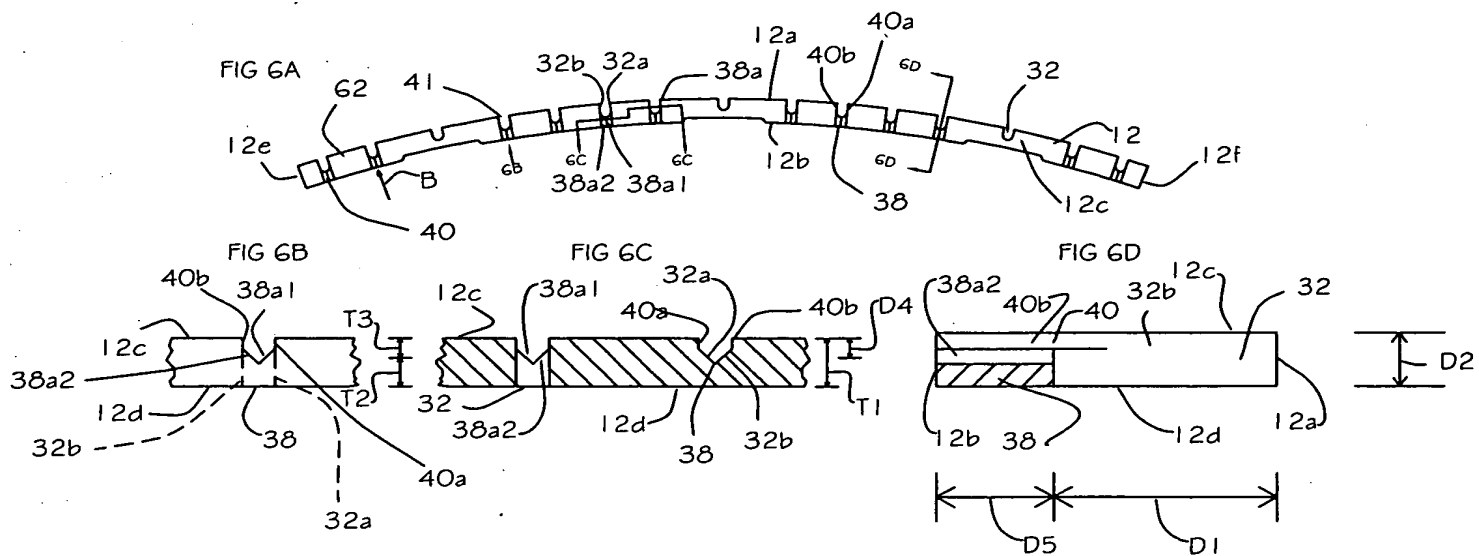
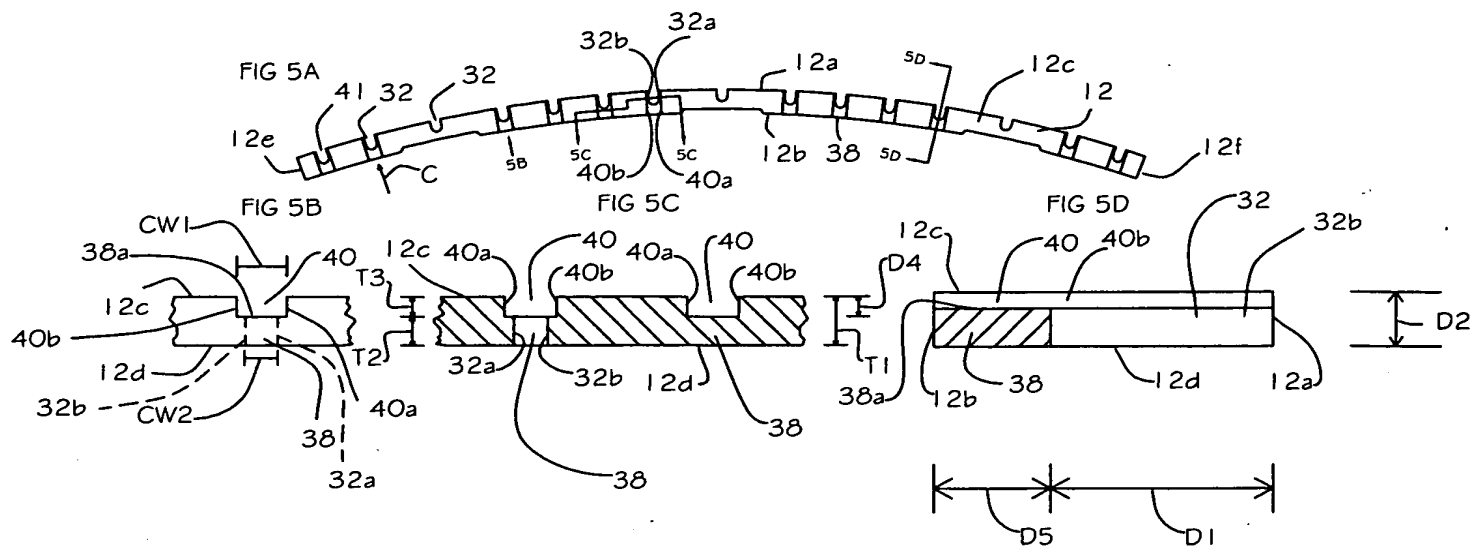
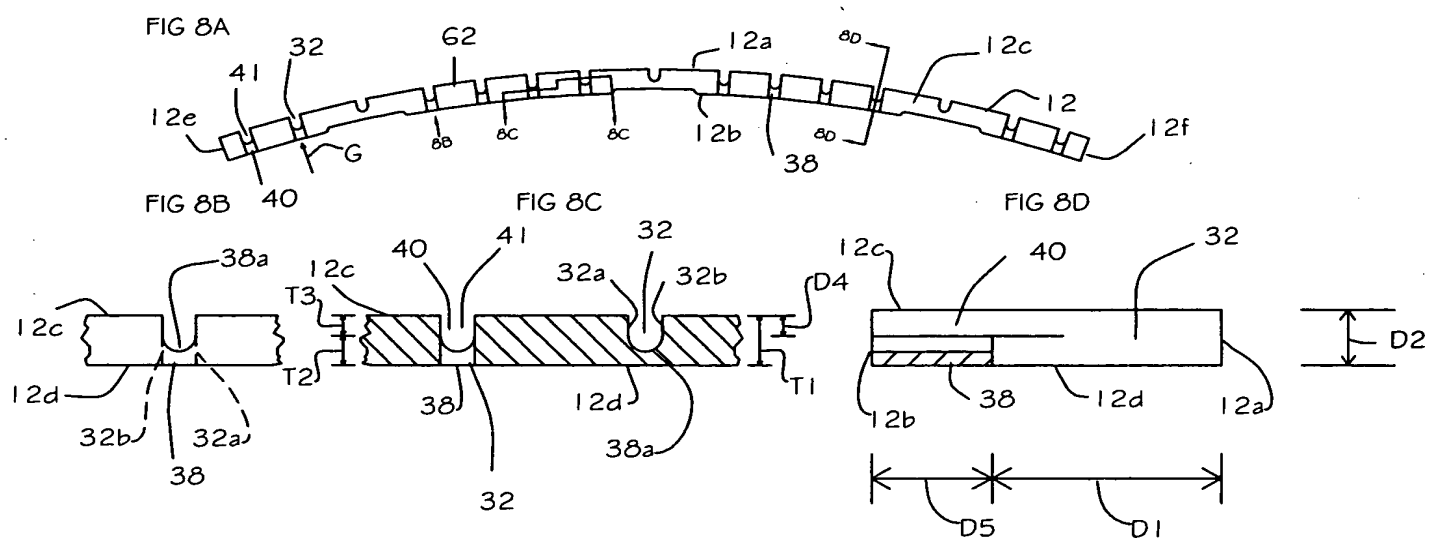
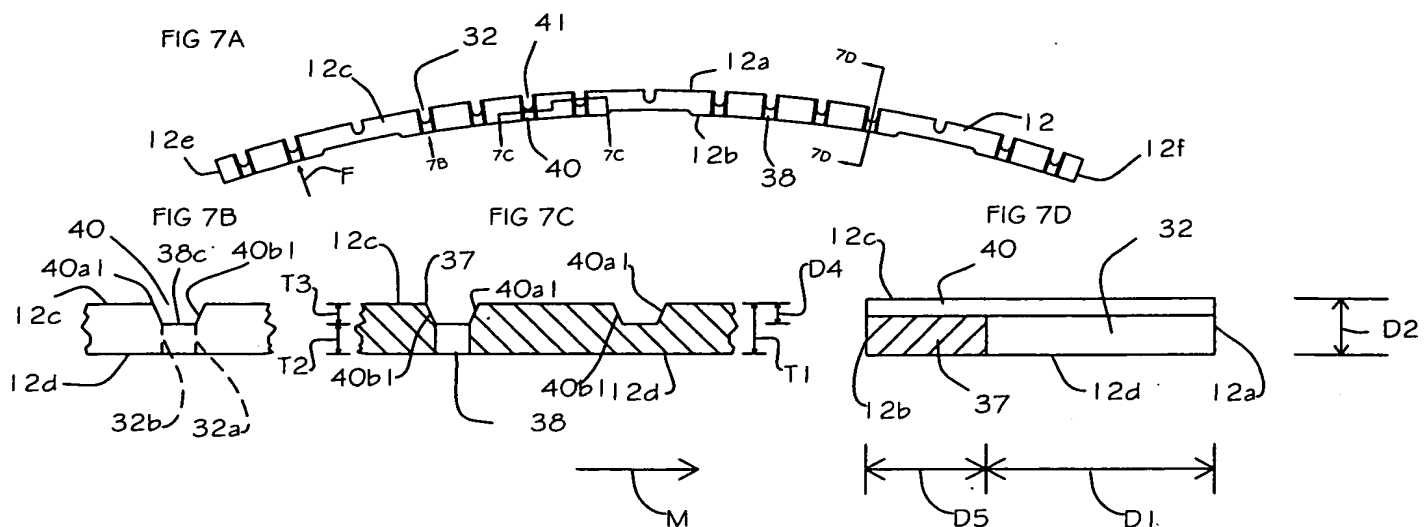


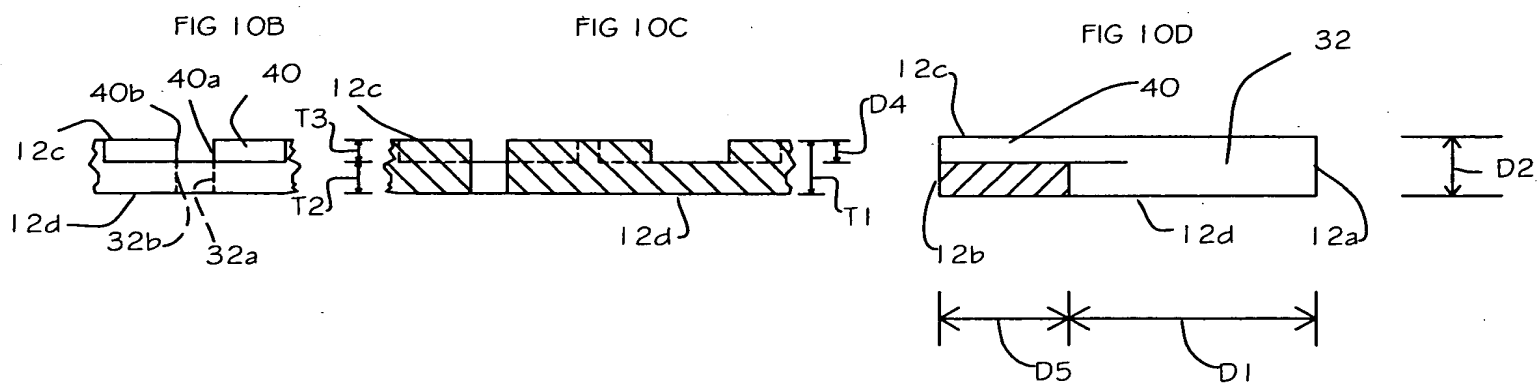
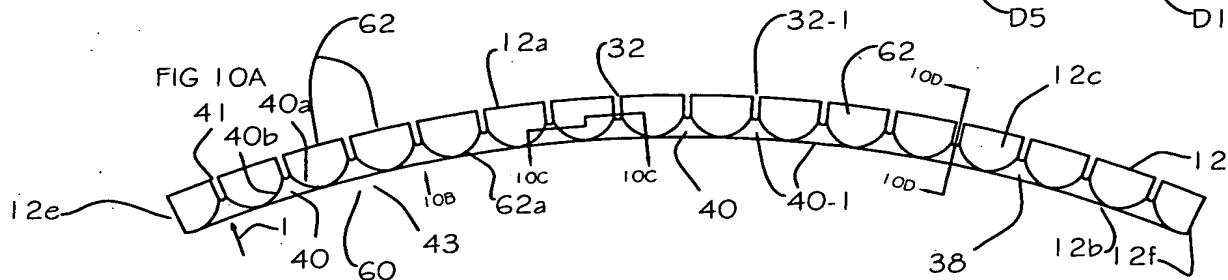
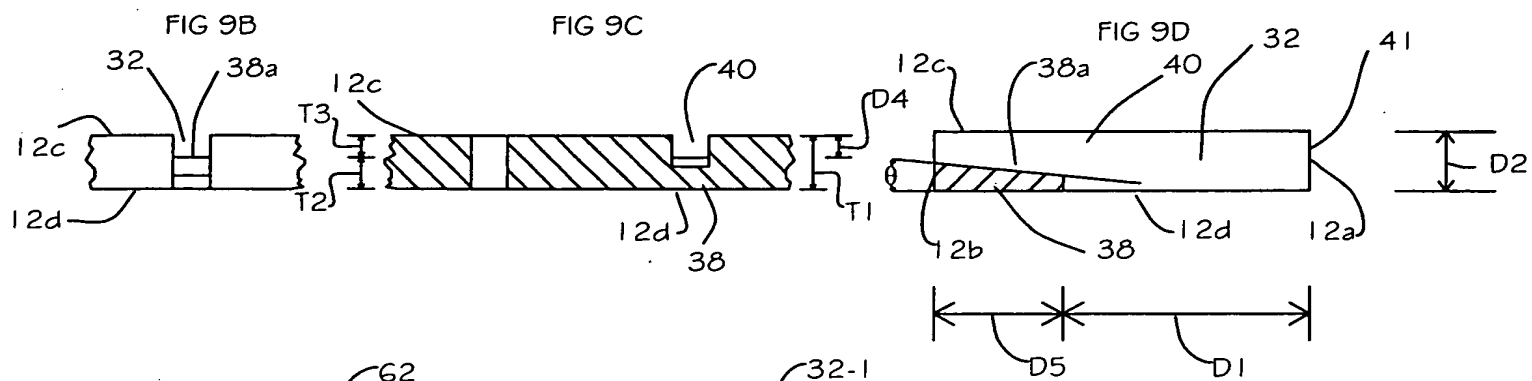
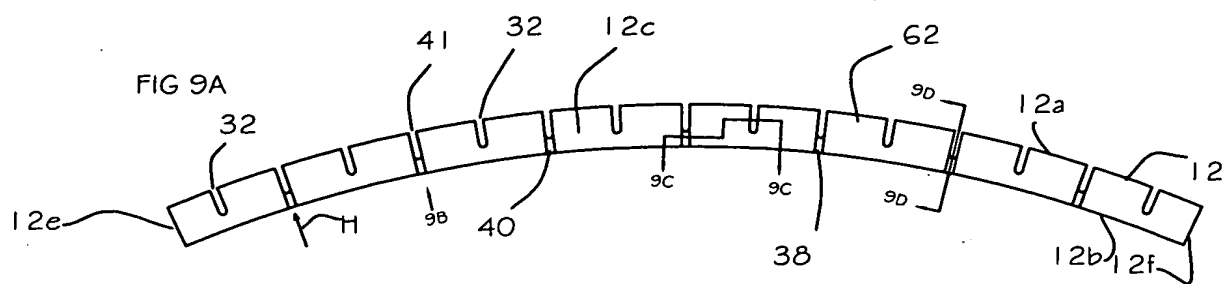
FIG 2

A cross-sectional view of a semiconductor device. It shows a substrate with a central region 12c and two side regions 12d. A layer 38 is formed on the substrate, and a layer 40 is formed on top of layer 38. The layer 40 has a central portion 40a and two side portions 40b. A layer T2 is formed on the substrate, and a layer T3 is formed on top of layer T2. The layer T3 is located between the central portion 40a and the side portions 40b.

FIG. 1 is a schematic diagram of a cable 10. The cable has a central core 12 with a central part 12a and two side parts 12b and 12c. The core is surrounded by a jacket 40 with a central part 40a and two side parts 40b and 40c. The jacket is divided into segments 32a and 32b by a joint 32c.







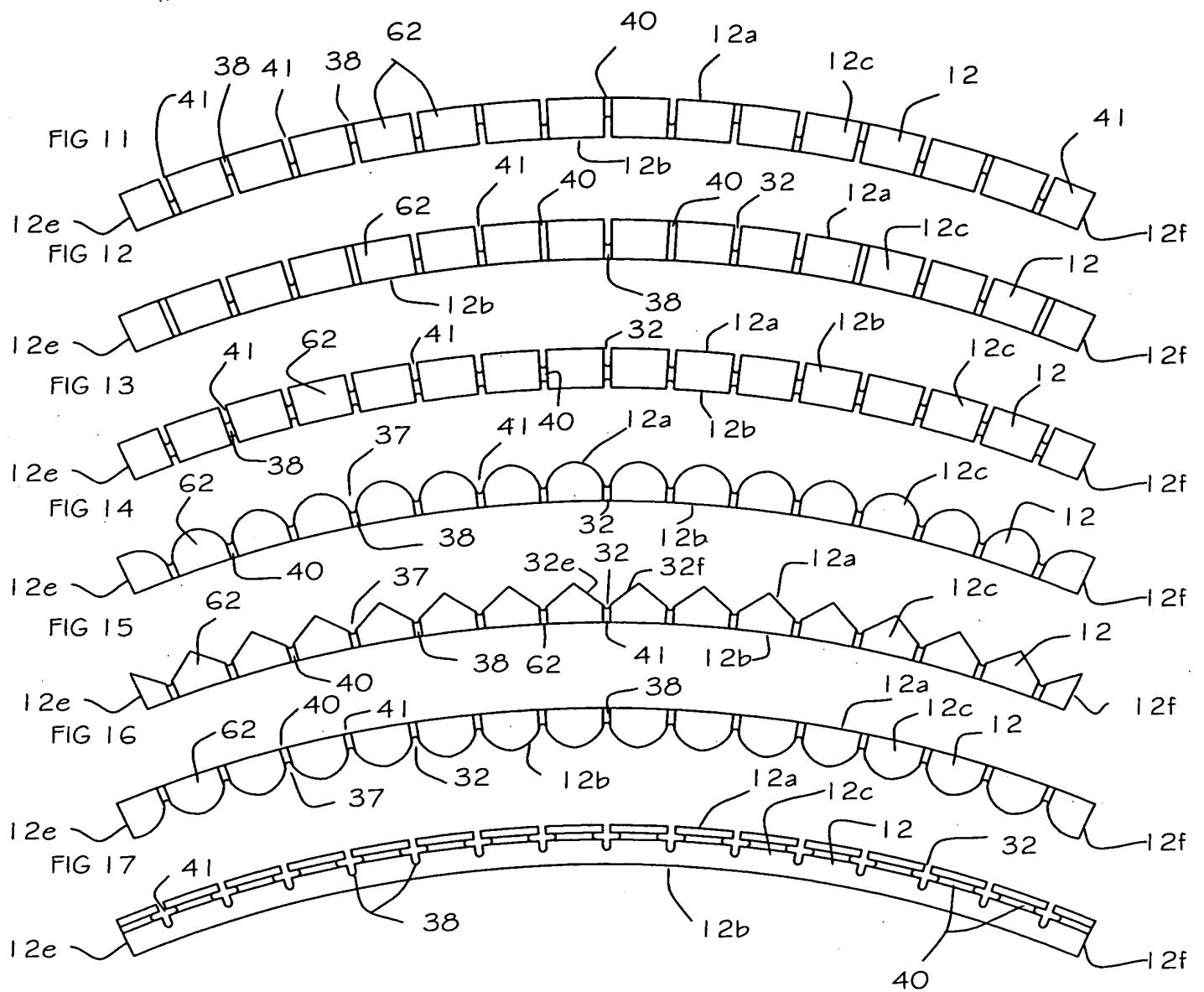


FIG 1B

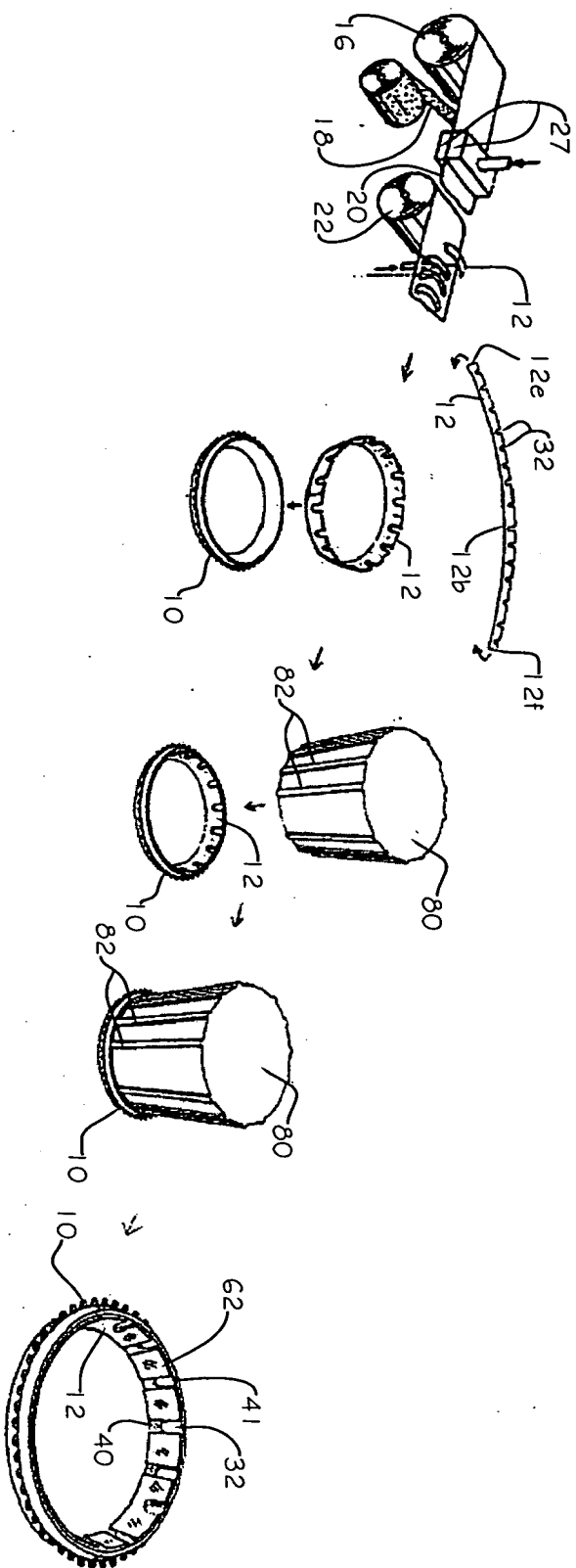




FIG 19

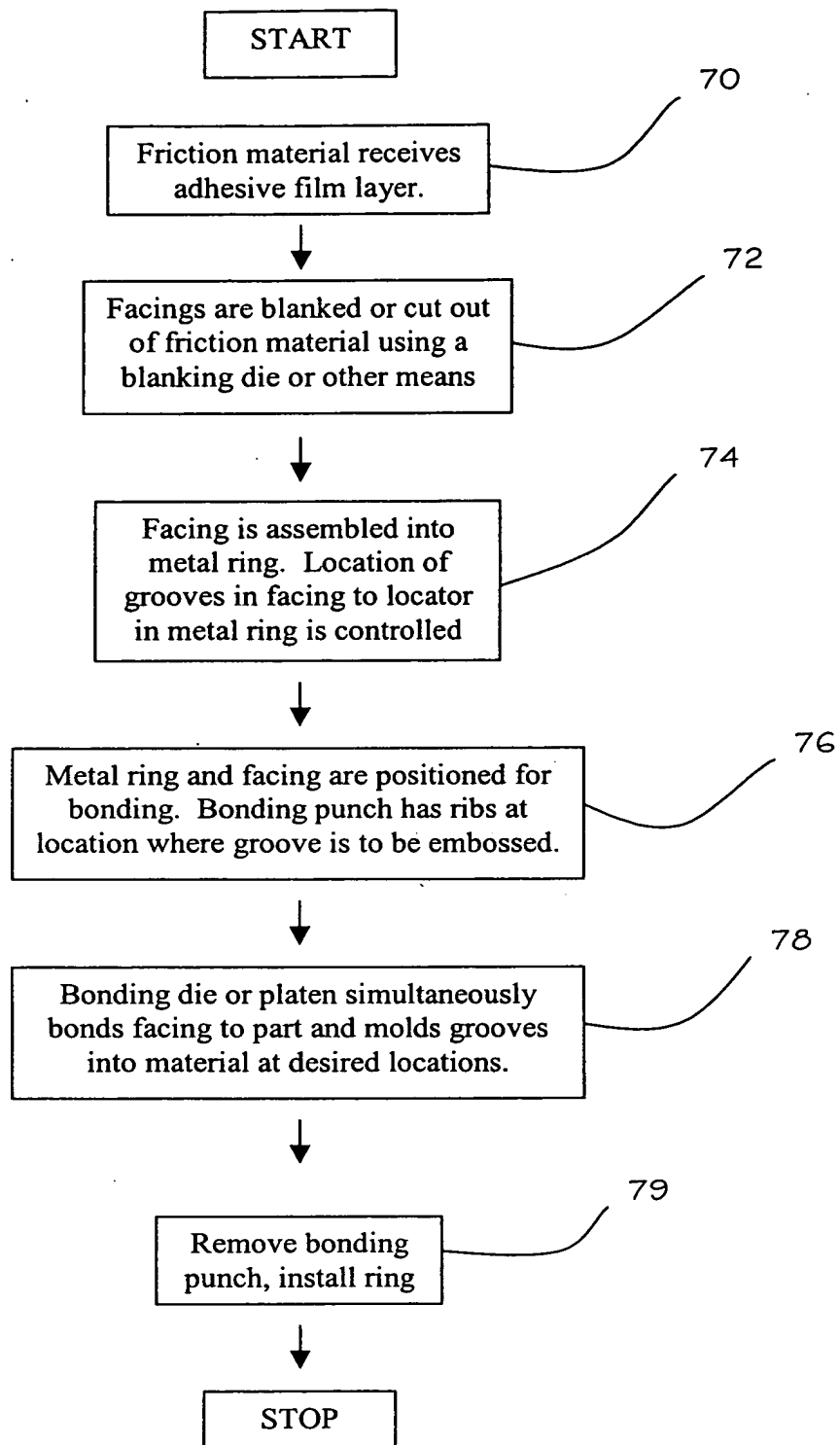


FIG 20A

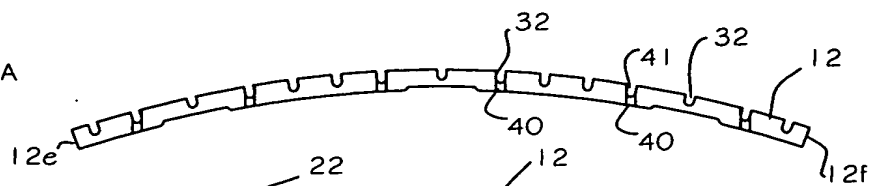


FIG 20B

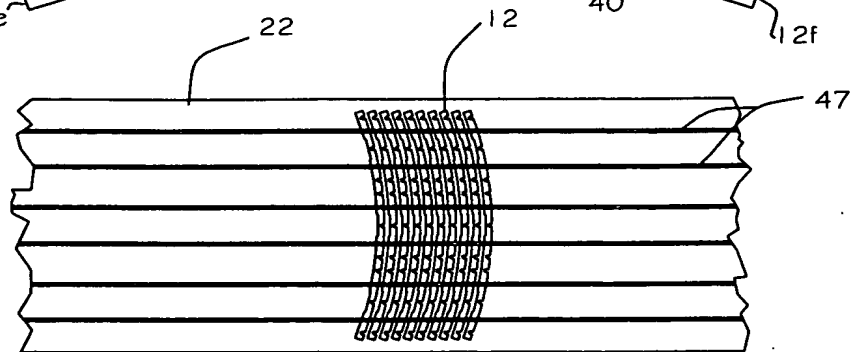


FIG 20C

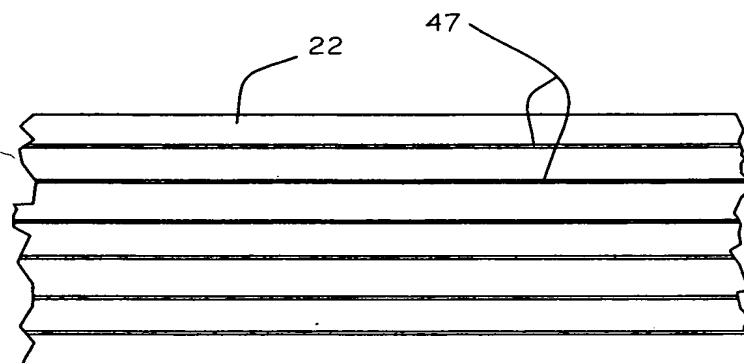


FIG 21A

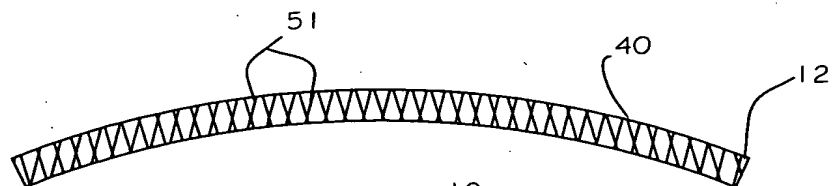


FIG 21B

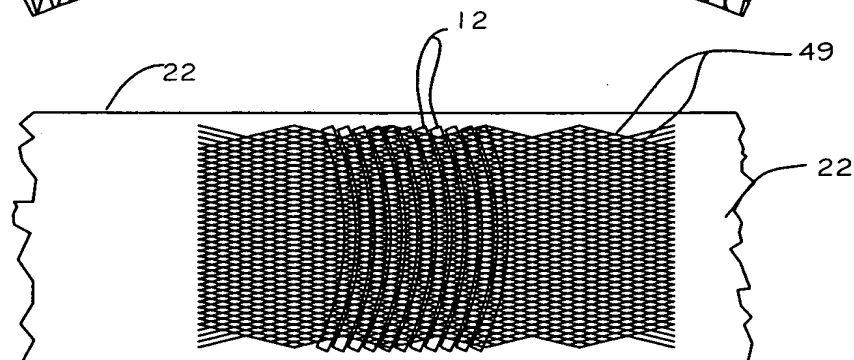


FIG 21C

